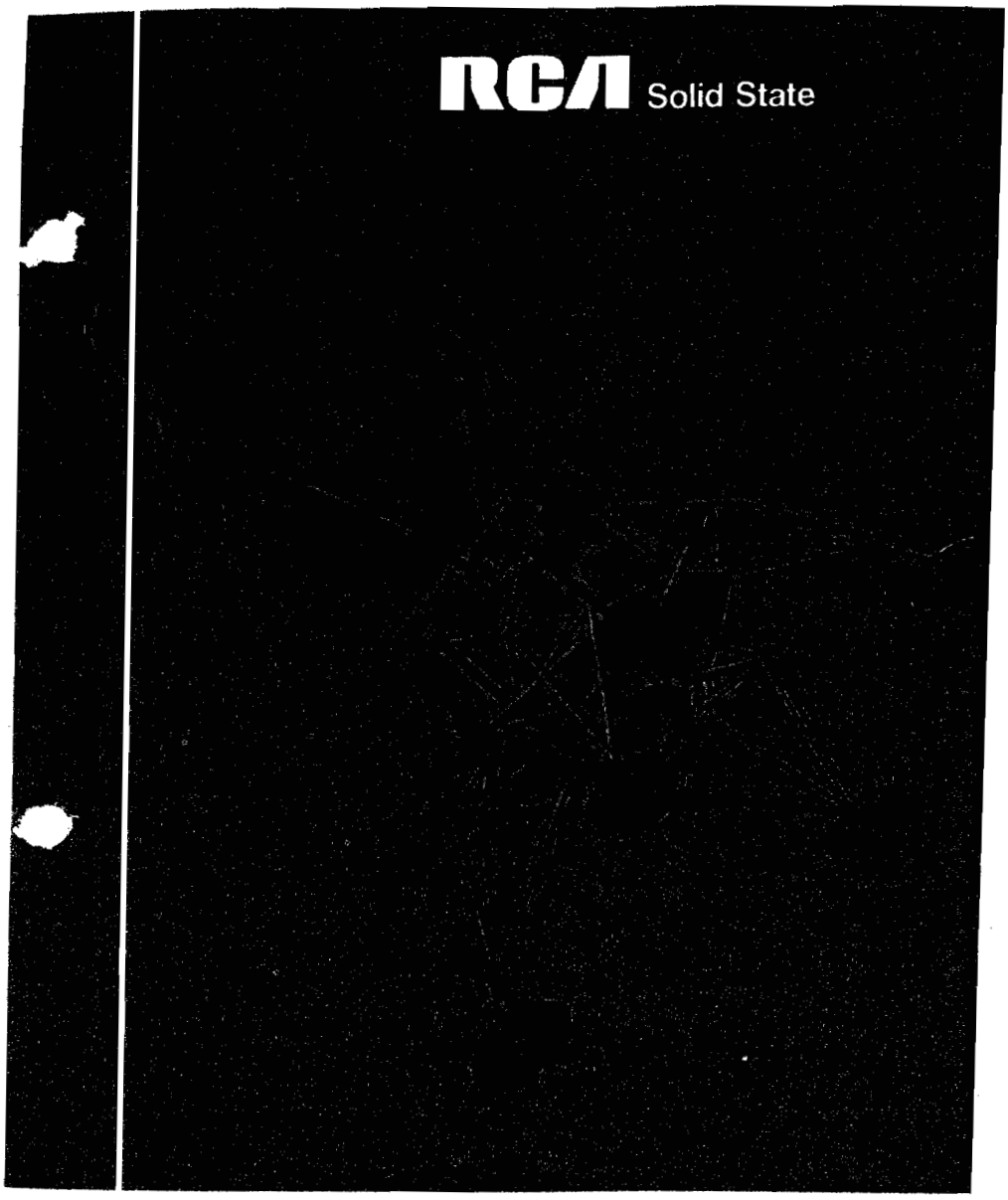
COS/MOS Application and Design Ideas



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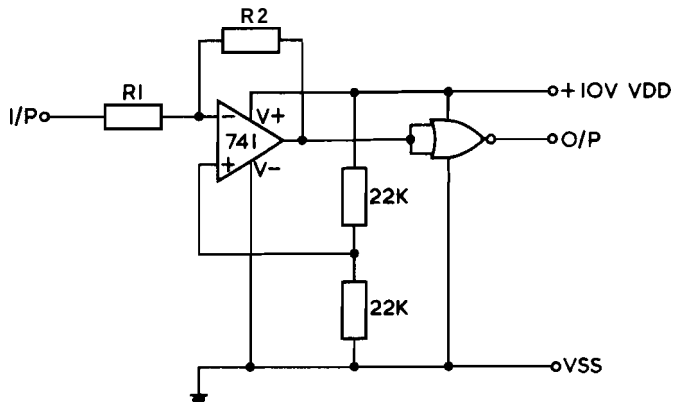
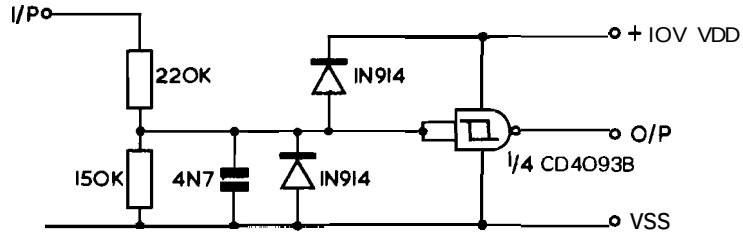
GS/3K/876 • Printed in England/8-76

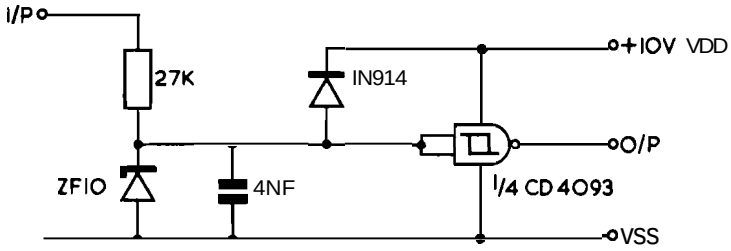
OP–AMP AND COS/MOS WITH COMMON SUPPLY RAIL



24V INDUSTRIAL LOGIC SWING TO COS/MOS INTERFACE CIRCUIT

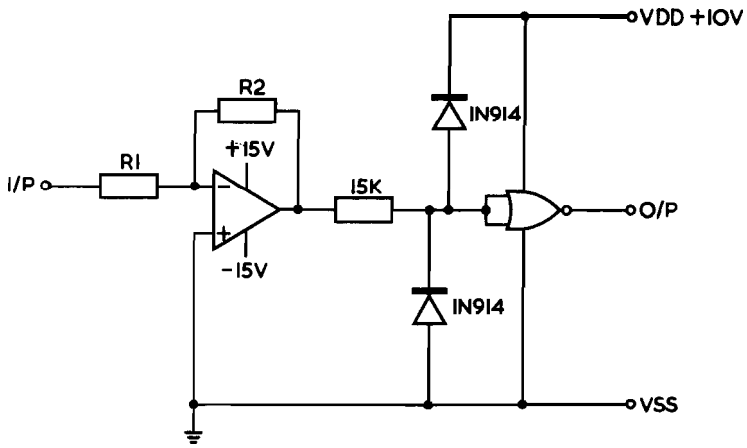


METHOD A



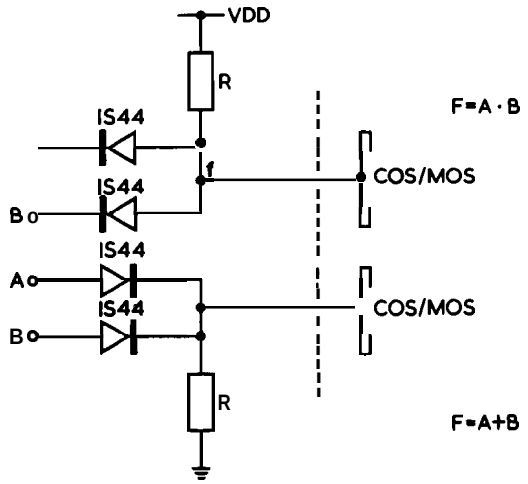
METHOD B

SPLIT RAIL OP–AMP TO COSIMOS INTERFACE

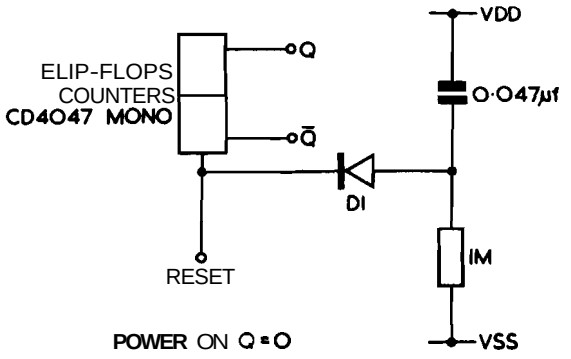


SIMPLE METHOD OF ACCOMMODATING EXTRA INPUTS TO COSIMOS CIRCUITS

R IS SELECTED FOR POWER–CONSUMPTION AND SPEED REQUIREMENTS



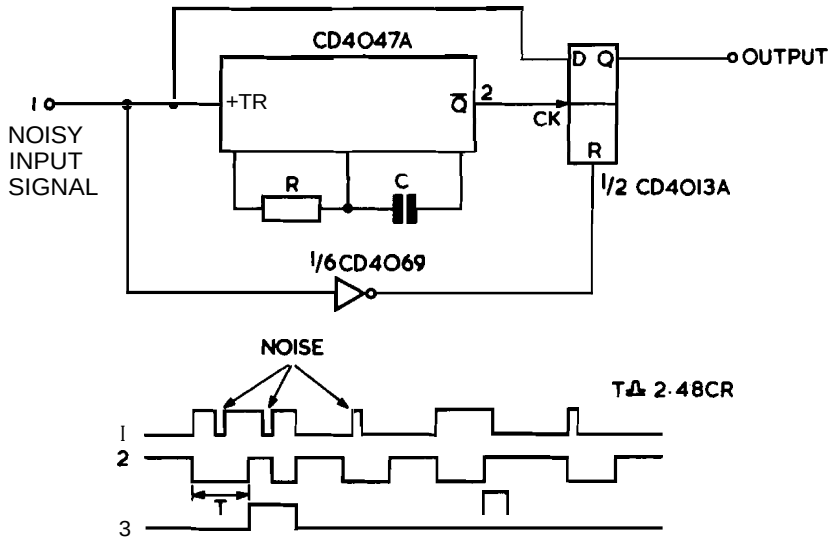
POWER-ON RESET CIRCUIT



Flip-flops, counters and circuits containing these elements are not guaranteed to reset when the supply voltage is applied. The above circuit shows a way of producing on automatic reset when power is turned on. This circuit is useful in connection with the **CD4047** monostable which contains a flip-flop in the output stage.

DI is included to isolate the **CR** network from any circuit connected to the reset input.

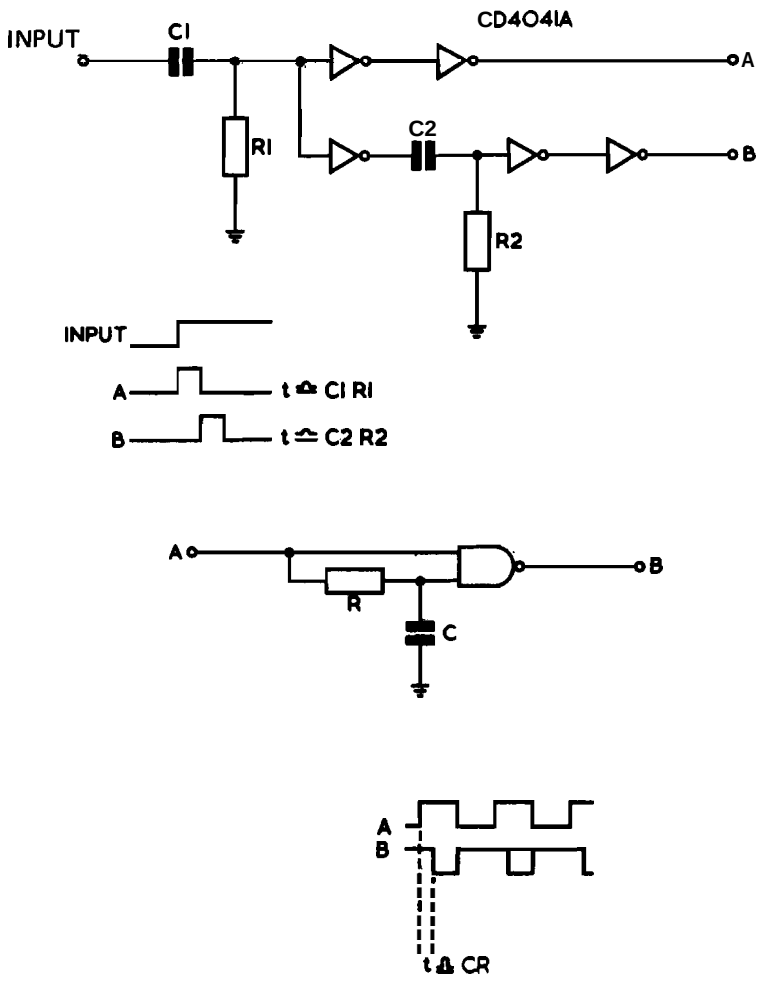
NOISE DISCRIMINATORS



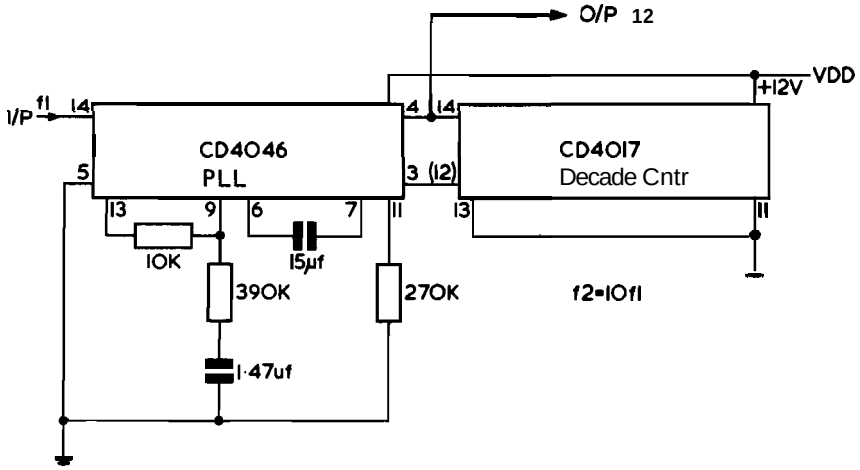
All input pulses with a pulse width shorter than that defined by the monostable time will not appear at the output.

The output will have its negative going edges coincident with the inputs. but will be reduced in pulse width by the monostable time. This circuit is useful in cleaning up transducer outputs, before being counted, so eliminating false counts due to noise spikes.

PULSE DELAYS ARE EASY WITH COS/MOS



DIGITAL FREQUENCY MULTIPLIER

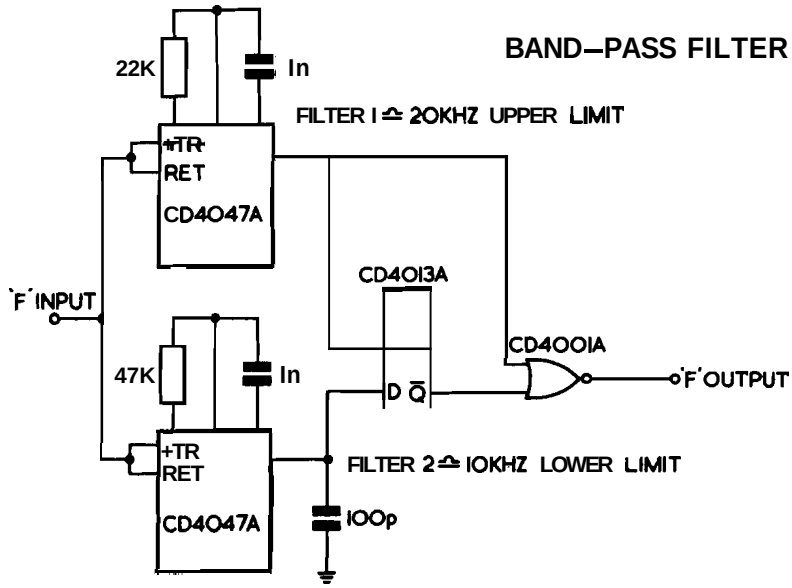


Multiplication factor :-

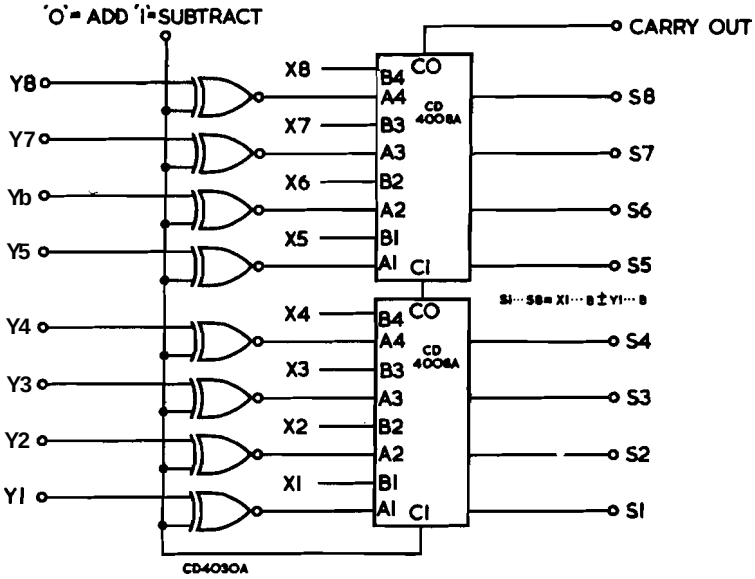
X9 connect pin 3 to pin	11 of **CD4017**
X8 connect pin 3 to pin	**9**
X7 connect pin 3 to pin	6
X6 connect pin 3 to pin	**5**
X5 connect pin 3 to pin	1
X4 connect pin 3 to pin	10
X3 connect pin 3 to pin	**7**
X2 connect pin 3 to pin	**4**
X1 connect pin 3 to pin	**2**

With the component values shown above the circuit will lock into input signals from 5Hz to 100Hz. Operation at other frequencies can be achieved by suitable choice of RC components in the phase locked loop. (See CD4046 data sheet and Application Note ICAN 6101).

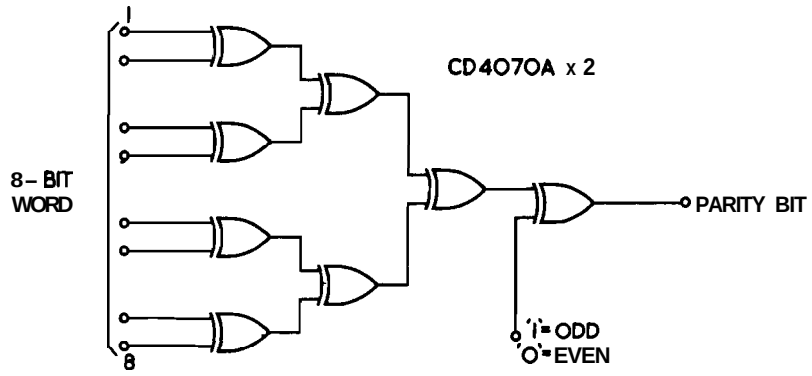
BAND–PASS FILTER



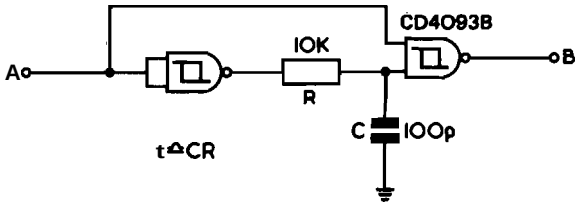
EIGHT–BIT ADDER/SUBTRACTER

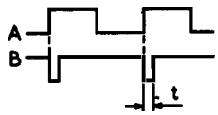


PARITY BIT GENERATOR

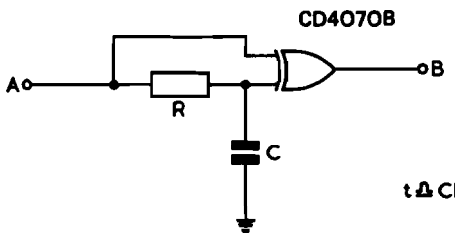


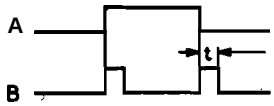
POSITIVE EDGE DETECTOR USING SCHMITT TRIGGER CD4093B



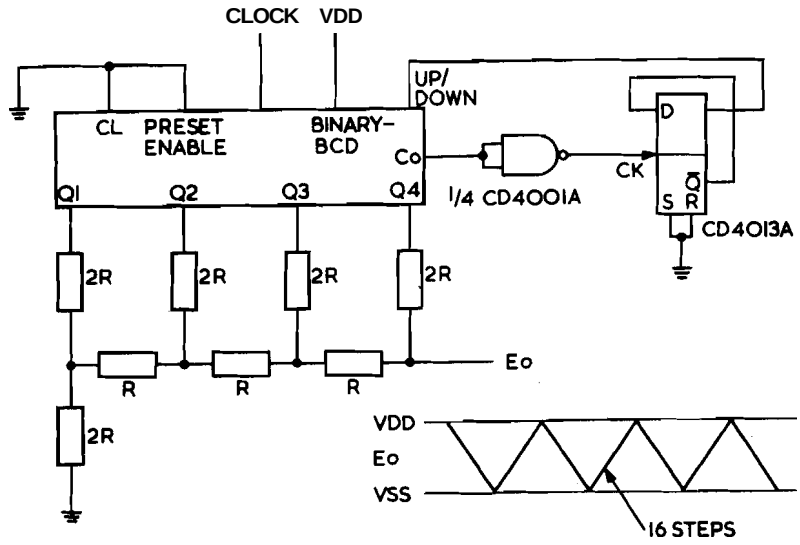


EDGE DETECTOR USING CD4070B

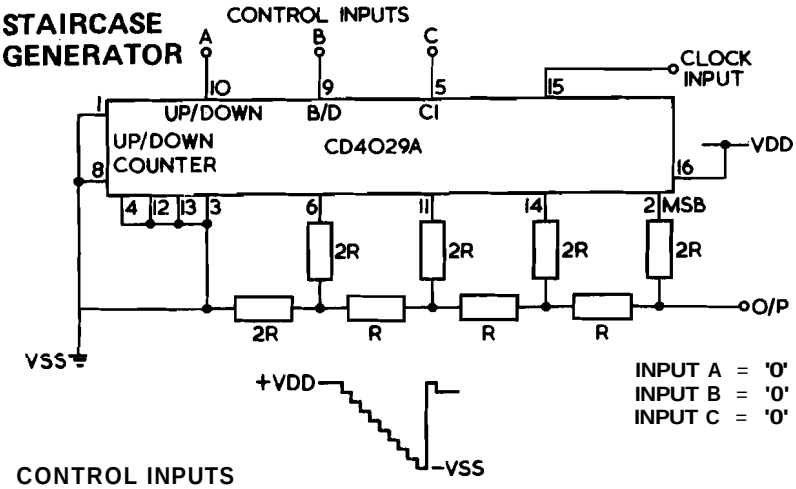




SAWTOOTH GENERATORS USING CD4029



STAIRCASE GENERATOR



INPUT A = '0'
INPUT B = '0'
INPUT C = '0'

CONTROL INPUTS

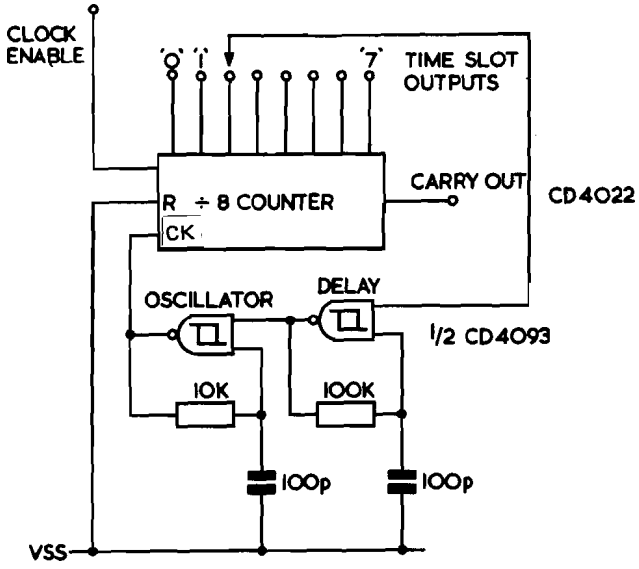
A = '0' RAMP DOWN
= '1' RAMP UP

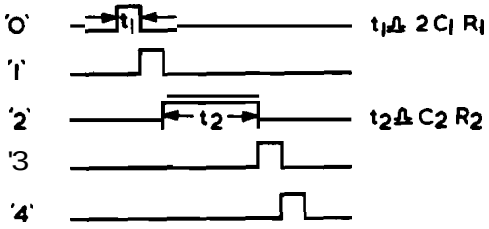
B = '0' 10 STEP RAMP
= '1' 16 STEP RAMP

C = '0' FREE RUN
= '1' STOP RUN

Suggested values for R = 100K

TIME SLOT EXPANDER



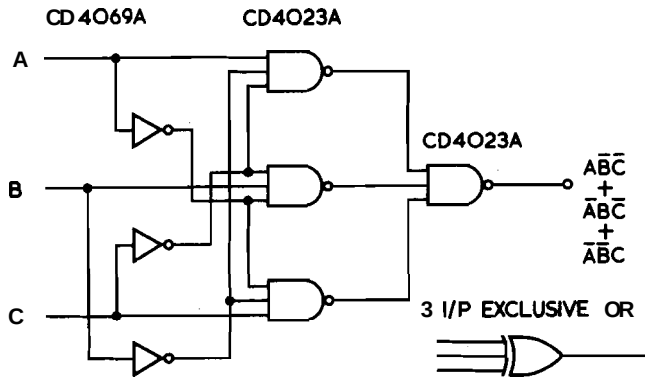


It is an advantage in some logic systems to carry out operations in a set sequence, controlled by a timing generator.

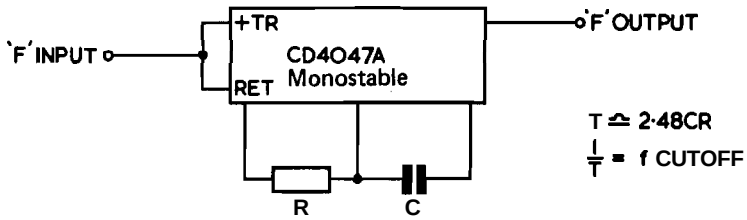
If a larger time slot is required, instead of gating together outputs and so reducing the slots available from the **CD4022** the pulse can be expanded by an amount' **R2 C2.**

By taking the clock enable input to a logic '1' the sequence can **be** arrested in any position.

3 I/P EXCLUSIVE OR GATE

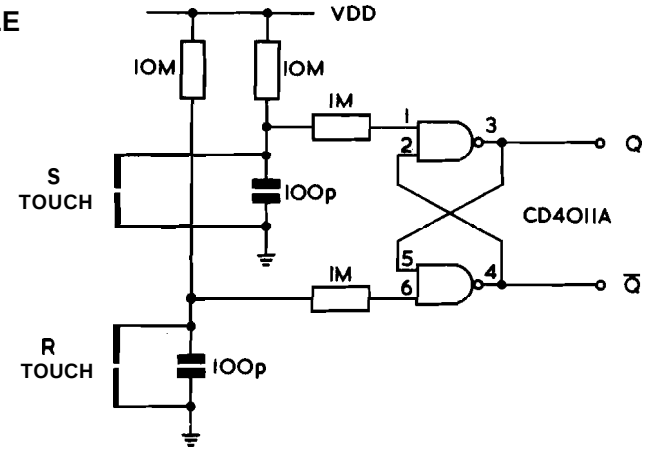


ACTIVE LOW-PASS FILTER



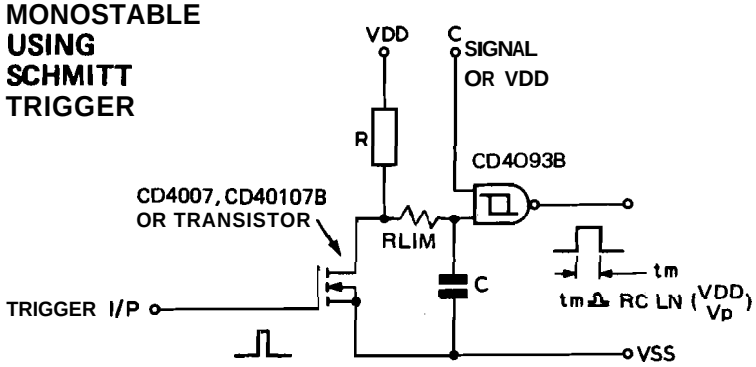
OUTPUT FOLLOWS INPUT FOR
FREQUENCIES LESS THAN F CUTOFF

TOUCH SET–RESET BISTABLE



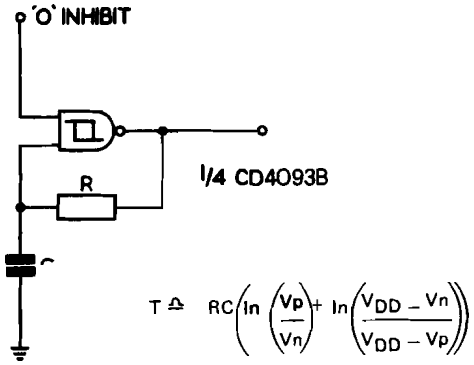
WHEN VDD = 10v CONTINUITY TOUCH
WHEN VDD = 5v PROXIMITY ACTIVATION

MONOSTABLE USING SCHMITT TRIGGER



If C is large a discharge current limiting resistor may be required when using the CD40107B. For safe area of operation, see Data Sheet. File No.

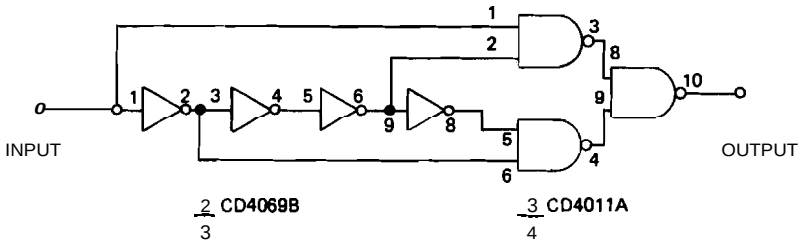
SCHMITT–TRIGGER OSCILLATOR



$$T \triangleq RC\left(\ln\left(\frac{Vp}{Vn}\right) + \ln\left(\frac{V_{DD} - Vn}{V_{DD} - Vp}\right)\right)$$

Vp and Vn = threshold voltages

PULSE FREQUENCY DOUBLER



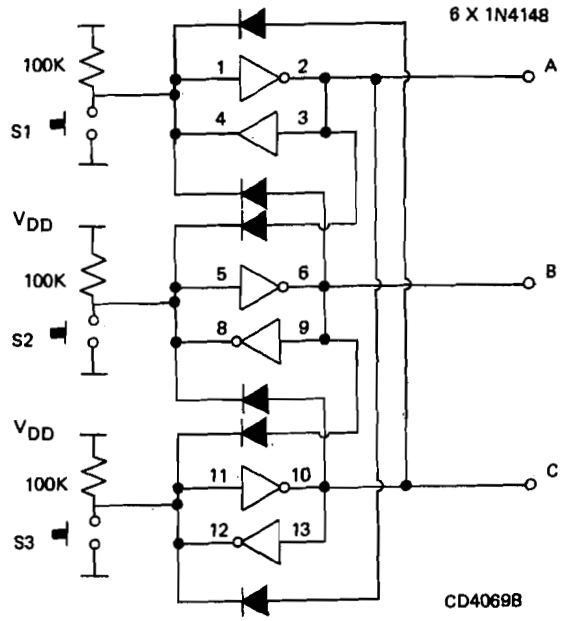
When a signal passes through the circuit each inverter introduces a small delay, typically 25 nS at 10V.

If the input is gated with the input's inverted form, appearing after the third inverter a pulse is produced three gate delays long after the positive transition of the input.

A pulse on the negative input transition is obtained in a similar way, one inversion step along the inverter chain. These two outputs are then added together to give a pulse at the output every logic transition at the input.

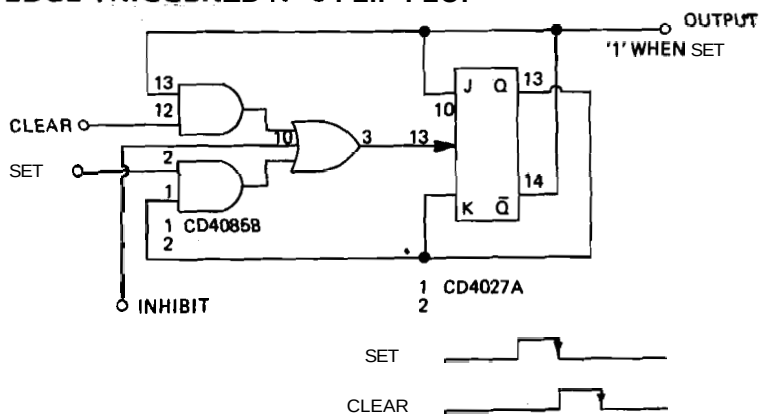
The circuit will operate up to ≈ 5.5 MHz at 15V and down to near DC if a Schmitt trigger is used at the input.

ANTI-BOUNCE PUSH SWITCHING



When switches S1, 2 or 3 are pushed a logic '1' is produced on the respective output and the remaining outputs reset to '0'.

EDGE TRIGGERED R–S FLIP-FLOP

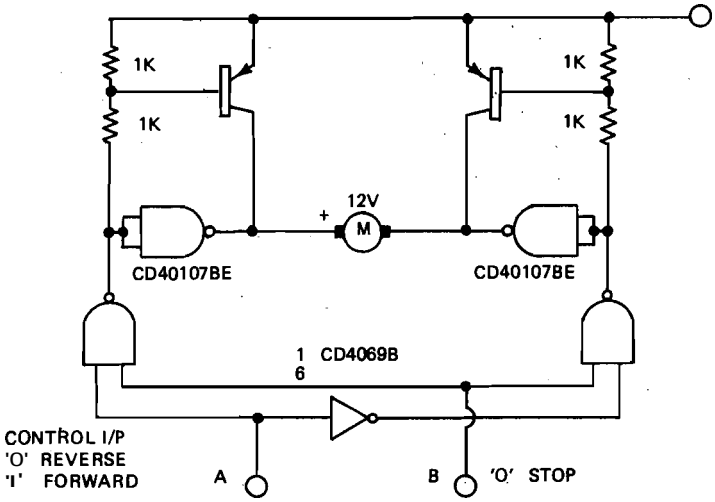


The use of an AND-OR-INVERT GATE with a J · K flip-flop enables expansion of the clock input.

Feeding the outputs of the flip-flop back to the inputs allows only a single output transition direction upon receipt of each successive clock pulse. This method makes the circuit operation independent of the initial state of the flip-flops. The outputs also select the earliest valid input signal for clocking the flip-flop.

A logic '1' on the inhibit input can be used to lock out the SET and CLEAR inputs.

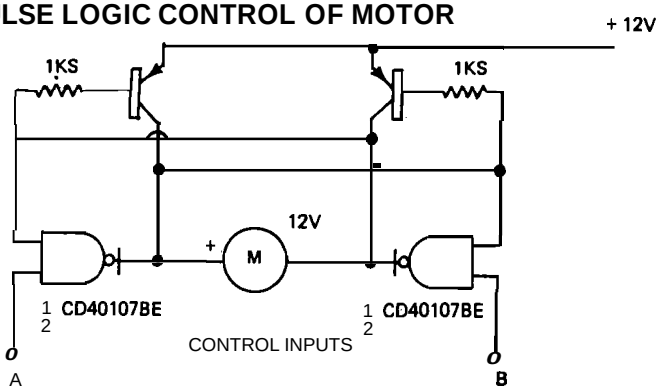
DC MOTOR CONTROL



With the addition of two PNP transistoo to the dual NAND buffer **(CD40107BE)** a complementary output drive is produced.

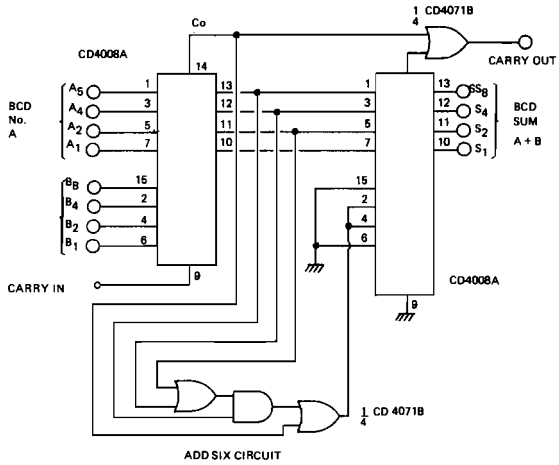
This is used to drive the motor in the forward or **reverse direction with** a logic input. The application of a logic **'O'** on **B** stops the motor **irrespectively** of input A, and **provides** a degree of dynamic braking.

CROSSCOUPLING ENABLES PULSE LOGIC CONTROL OF MOTOR



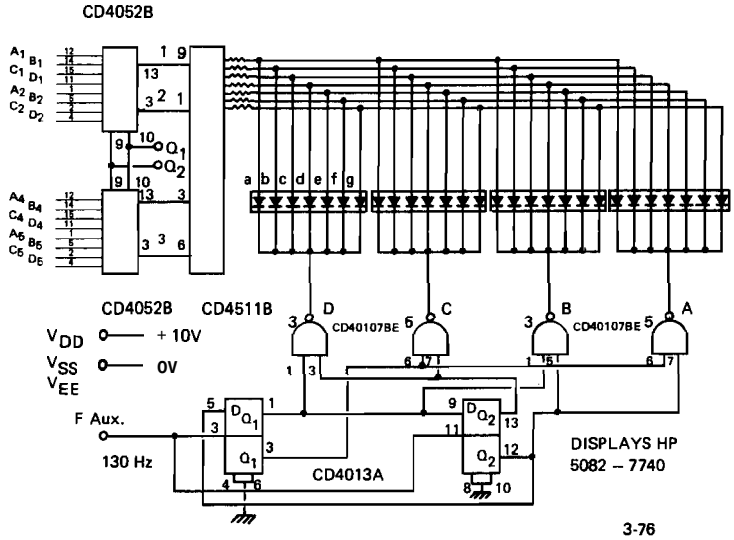
A	B	MOTOR FUNCTION
0	0	OFF
1	0	COUNTER CLOCK-WISE
1	1	AS PREVIOUS STATE
0	1	CLOCK-WISE
1	1	AS PREVIOUS STATE

4-BIT FULL BCD ADDER



To add two BCD numbers with ordinary full binary adders, a six is added f a sums that are greater than nine. This circuit can also be used to convert a 4-bit binary number to BCD. In this case the first adder is not needed, and the Co. input to the add-six circuit is also eliminated.

4-DIGIT DISPLAY MULTIPLEXER WITH BCD INPUTS



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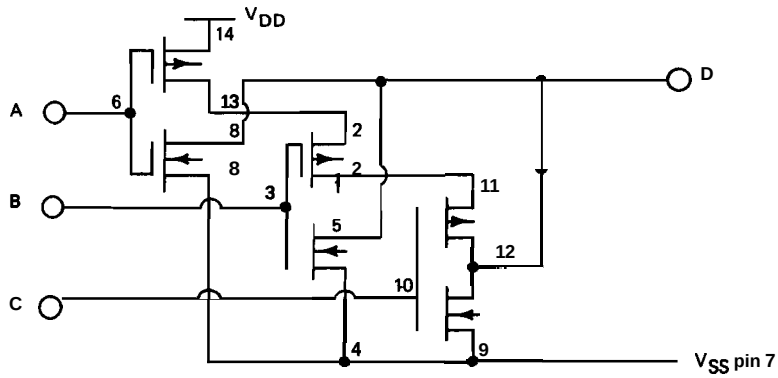
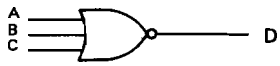
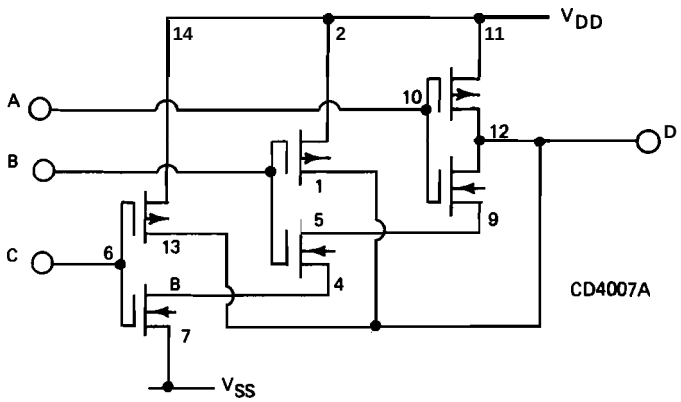
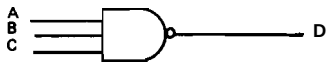
LOGIC FUNCTIONS USING THE CD4007A





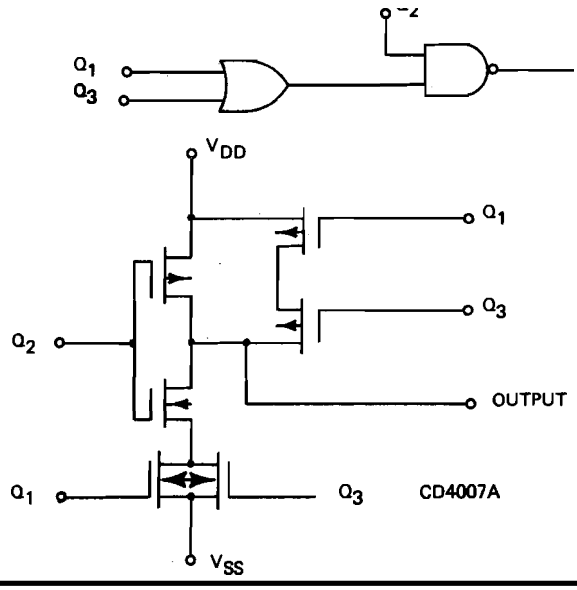
THREE INPUT NOR GATE





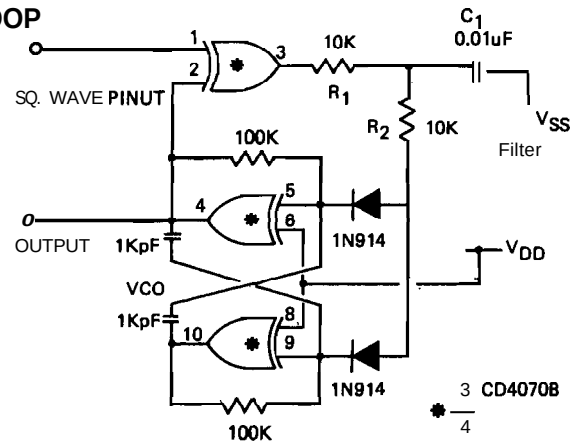
THREE INPUT NAND GATE

COMBINATIONAL LOGIC



CD4007 Pin Connections
(2, 13) (5, 4, 9) (1, 12)
(11, 14) (4, 7)
Output pin **12**
Q1 = pin **6** Q2 = pin **10**
Q3 = pin **3**

PHASE-LOCKED LOOP USING EXCLUSIVE OR GATES



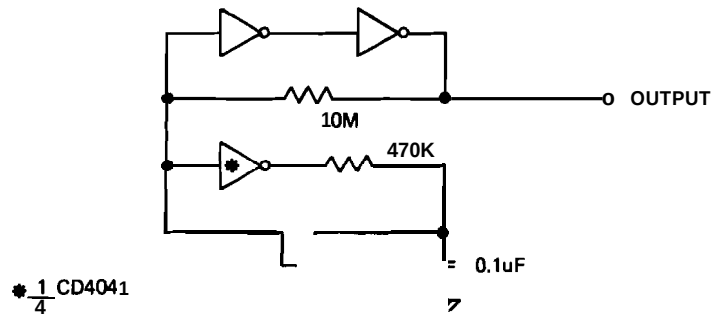
A complete phase-locked **loop** circuit, which **includes** a VCO, phase comparator and filter, can be made from **three-quarters** of a **CD4070B** EX - OR Gate.

The circuit produces a square-wave output in quadrature with the input signal. The lock and capture ranges are determined by the valuer of the filter, R_1, R_2 and C_1.

For the circuit shown, the center frequency is nominally **10KHz.** The loop can capture the input frequency over better than a 1.5 : 1 range and track over a 4 : 1 range.

The loop will also lock to input signals that are multiples of the VCO frequency.

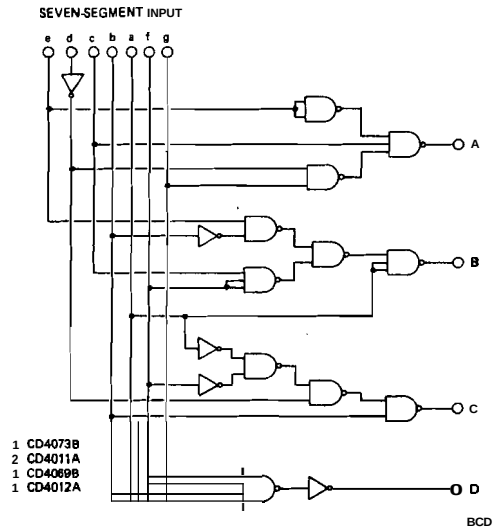
TOUCH SWITCH WITH LATCH



TOUCH CONTACTS

The circuit is switched by making a conductive path with the fingers across 2 contacts.
The circuit will remain in the new state until contacts are made again.

SEVENSEGMENT TO BCD DECODER

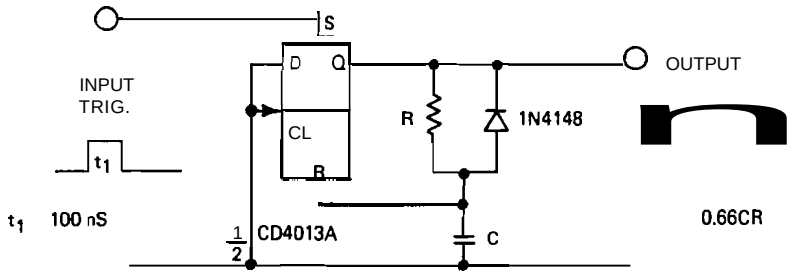


BCD

	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	1	1	0	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1

CD4013A USED AS A MONOSTABLE



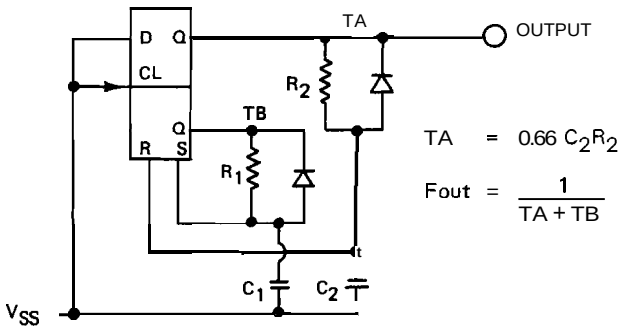
R range – 27K – 10M

C range – The lower limit is determined by the flip-flop's minimum reset pulse width, which is about 125nS at 10V - (5oonS at 5V). A typical value for C is 0.033uF. The upper limit can be quite large so long as the discharge current into the output does not exceed the package dissipation.

A reset during the timed period can be accomplished by raising the clock input to a logic '1'.

CD4013A USED AS AN ASTABLE

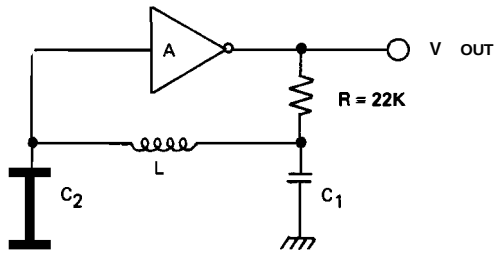
R. & C. Range limitations as for monostable.



$$TA = 0.66\ C_2R_2$$

$$Fout = \frac{1}{TA + TB}$$

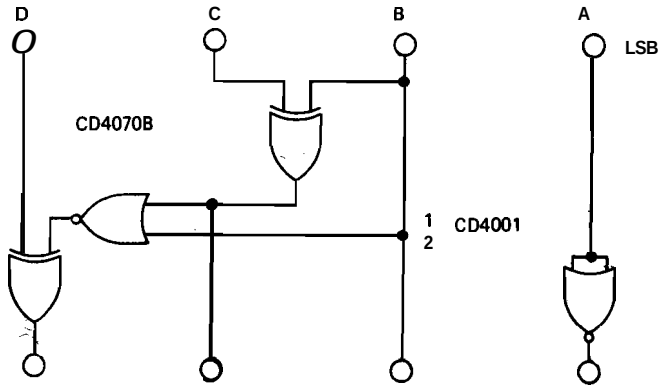
COS/MOS LC OSCILLATOR



$$F = \frac{1}{2\pi\sqrt{L\,\frac{C_1C_2}{C_1+C_2}}}$$

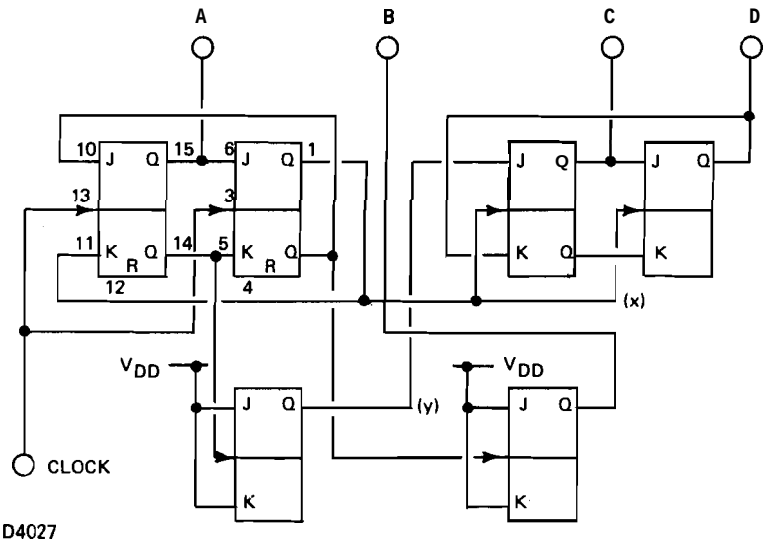
IN PRACTICE $C_1 = C_2$

BCD TO 9'S COMPLEMENT LOGIC



9's COMPLEMENT OUTPUT

4-BIT GRAY CODE COUNTERS

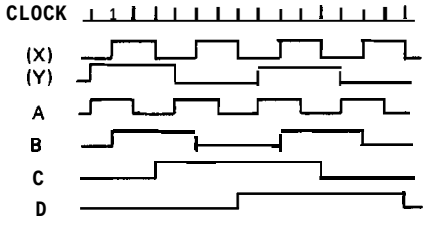


3 X CD4027

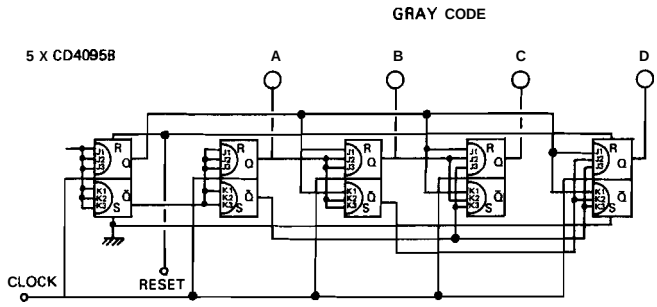
When binary signals are AND ed together, undesirable glitches can be generated at the output.

The output lines of these Gray-code generators have no simultaneous signal transiston permitting them to be AND ed together without creating glitches

For correct operation all bistables must be reset initially.



HIGH SPEED GRAY CODE COUNTER

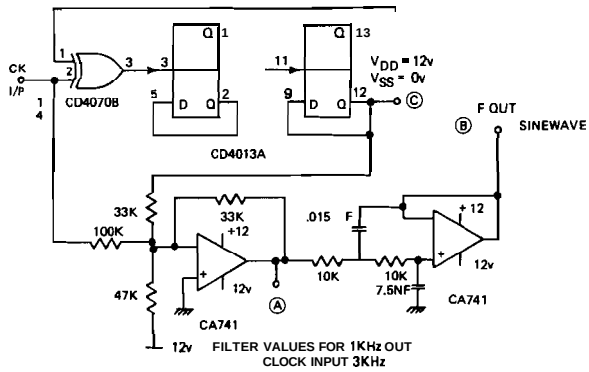


CD4095B – MAX TDGGLE FREQUENCY TYPICALLY 16 MHZ AT 10V V_{DD}

THE GRAY CODE

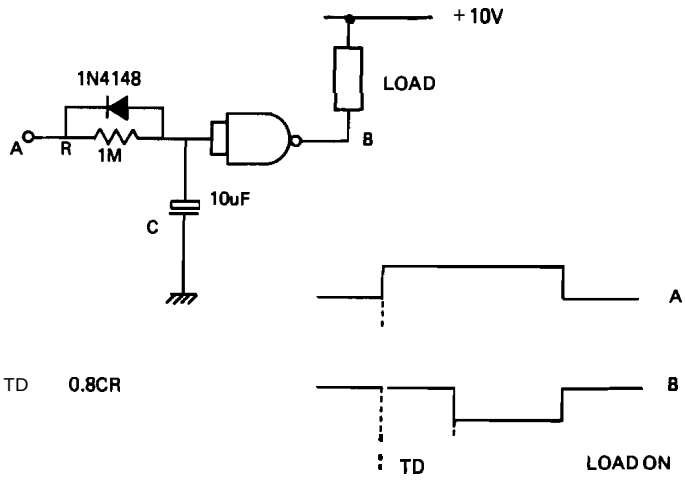
	A	B	C	D		A	B	C	D
0	0	0	0	0	9	1	0	1	1
1	1	0	0	0	10	1	1	1	1
2	1	1	0	0	11	0	1	1	1
3	0	1	0	0	12	0	1	0	1
4	0	1	1	0	13	1	1	0	1
5	1	1	1	0	14	1	0	0	1
6	1	0	1	0	15	0	0	0	1
7	0	0	1	0	16	0	0	0	0
8	0	0	1	1					

DIGITAL SINE-WAVE APPROXIMATION



The output on (A) approximates to a sine-wave, the first harmonic of which is five timn the fundamental. The low-pass filter shown provides a better sine-wave at (B) if required.

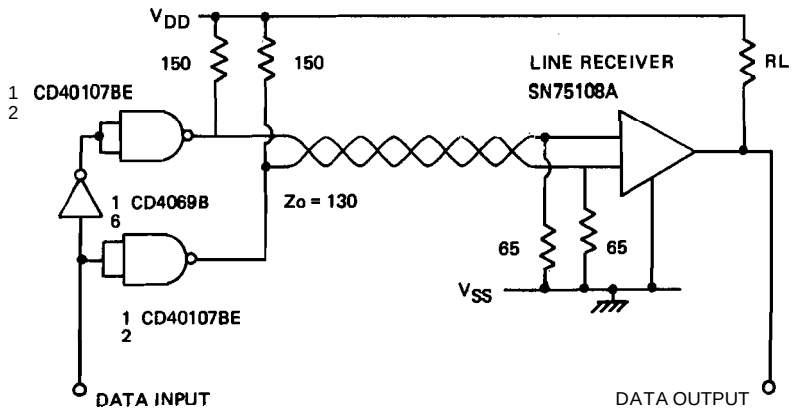
DELAYED LOAD SWITCHING



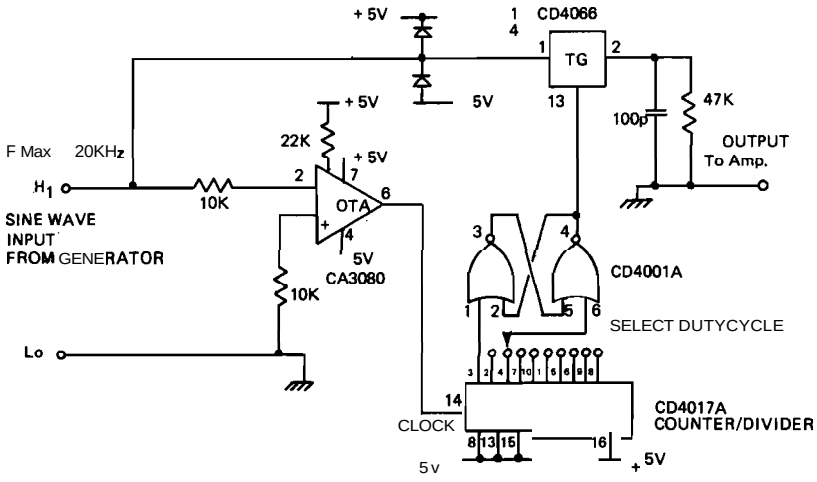
This circuit will give a delay to the switching of the load, after a logic '1' has been applied to the input.

Due to the high gain of this buffer below about 12 volts, long time constants can be used whilst maintaining an abrupt output transition.

LINE DRIVING



CYCLE DELETION

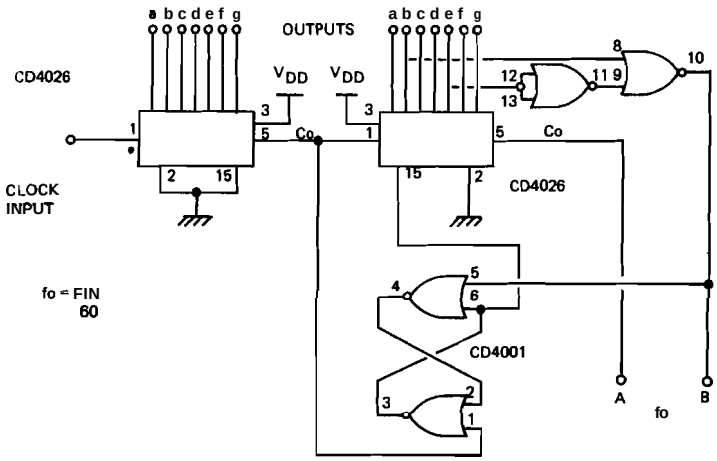


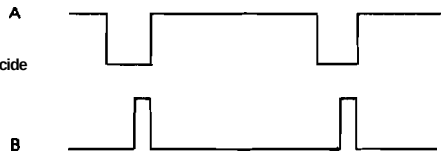
DUTY CYCLE

Cycles deleted out of 10	Pin No. CD4017
1	11
2	9
3	6
4	5
5	1
6	10
7	7
8	4
9	2

This circuit can provide a more realistic way of testing audio amplifiers on load. At full output swings a continuous sine wave can cause undue power dissipation or supply voltage drop.

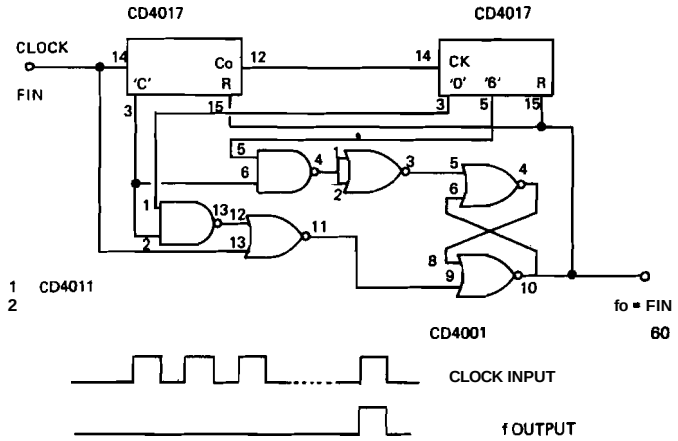
DIVIDE BY 60 WITH 7-SEGMENT OUTPUTS



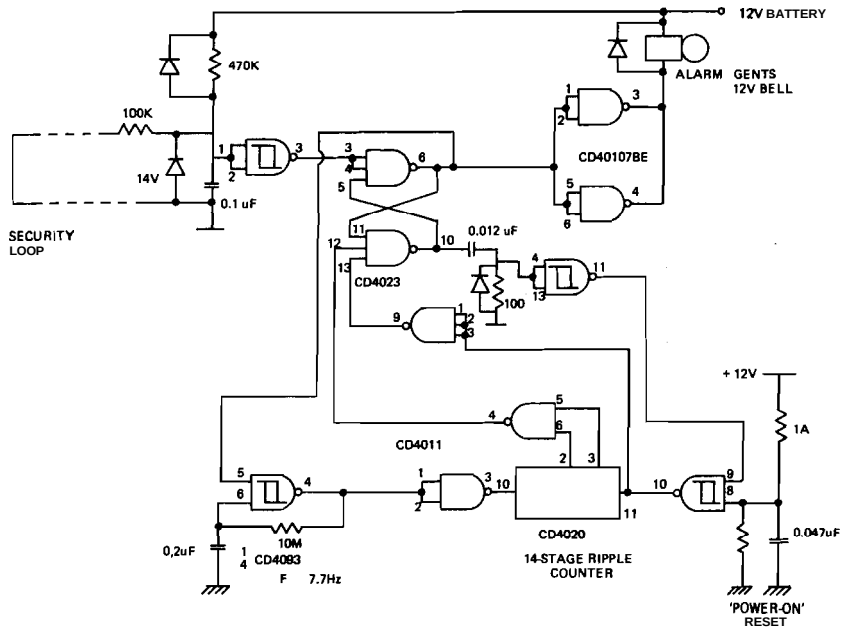


The clock input's positive edges coincide with the edges at output A and B.

DIVIDE BY 60



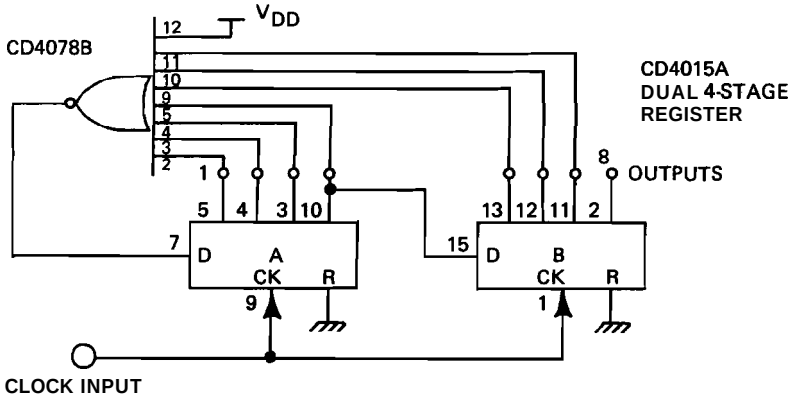
LOW STAND-BY POWER ALARM SYSTEM



When an open circuit occurs in the security imp the latch, a cross-coupled 3-input NAND gate, is set, which enables the alarm. This will remain set even *it the* loop is now completed.

The CD4020A 14-stage ripple counter is clocked by e slow running oscillator, to produce an output signal to reset the latch after about 25 minutes and turn off *the* alarm. The alarm will only remain on if the loop remains open circuit.

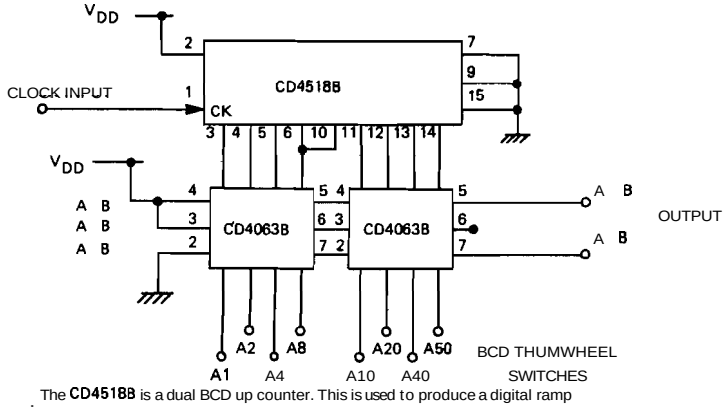
CIRCULATING SHIFT REGISTER



Every clock period a logic 'I' is stepped along the eight outputs in sequence.

Alternatively a 'O' can be obtained by changing the NOR gate to a NAND gate (CD4068B) and returning pin 12 to V_{SS}.

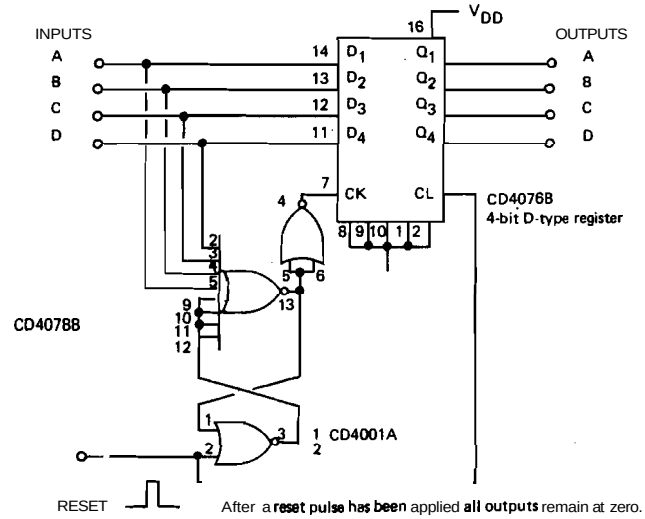
DIGITAL CONTROLLED PULSE WIDTH MODULATOR



The CD4518B is a dual BCD up counter. This is used to produce a digital ramp at ia output when supplied with clock pulses.

When this output is compared with a selected digital value by a pair of magnitude comparitors CD4063B's, a pulse is obtained at A B output that can be incremented from one clock period in width 1%dufy cycle, to 100% dufy cycle. The A B output appears as an inverted form of A B.

TIME – PRIORITY 4-CHANNEL LATCH



After a reset pulse has been applied all outputs remain at zero. A pulse that occurs on any input line sea the bistable, which causes a positive transition at the clock input of the CD4076B. This edge clocks Ihe data through to the respective Q output.

If any other pulses occur on the input lines after this pulse they will fail to clock the bistable and in consequence wilt not be transferred to the output. Thus the four output lines will record which pulse was received first.

COS/MOS Application and Design Ideas